A Unique Semiconductor ATE Reprogrammable System Hardware
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1. Corporate Information
Corporate Information

- Market Research
- Product Marketing
- Sales & Sales Support
- Project Management
- Account Management
Corporate Information - Focus & Capabilities

Total solutions for
- Test
  * Sockets, Probe Cards, Bed of Nails
- Handling
  * Device handler, Wafer prober
- Application
  * Project, Software & Hardware set up
- Burn In
  * Project, Driver and BiBoard

PCB/Modules - InCircuit Test, Functional Test and Repair
High Power Discretes - Static, dynamic and constant test of IGBT, Transistors, FET, Thyristors, Diodes, Modules
SoC mixed signal - µController, Asics, analog and digital IC, FPGA, Memory
MEMS - like SoC including physical manipulation 3D Gyroscope, Accellerometer, Pressure sensors
RF - High frequency devices & modules
2. Product Information

The M-Platform
SoC Semiconductor Testsystem

HIGH PERFORMANCE for low entry cost

- Dynamic digital test up to 1600 MHz
- Parameter measurement per channel
- Analog digitizer 24Bit@250kS & 16Bit@250MS
- Analog waveform generator 16Bit@400Msteps
- Mixed signal test of SoC (System on Chip) and 3D chips
- Memory test of DRAM, RAM, Flash, Eflash etc.
- Handler and Waferprober interface
- MEMS test including Handler and Manipulation
- Engineering tester for software development
SoC Semiconductor Testsystem

History

- Engineering team historically from Schlumberger (*SENTRY15, ITS9000, SAPPHIRE-Platform*)
- Following IPO of test division, acquisition, shutdown of French plant by Credence in 2008
- Company founded in 2009, close to St Etienne – France, benefiting from leading IP & know-how in FPGA based hardware & software semiconductor test
- New test platform launched end of 2011
SoC ATE revolutionary architecture

32 ASICs replaced by 1 FPGA
Dramatic optimization of memory resources

Traditional ATE architecture

- ASIC Memory Tester Channel
- ASIC Memory Tester Channel
- ASIC Memory Tester Channel
- ASIC Memory Tester Channel

MuTest IP and revolutionary architecture

- System cost divided by at least 3,
- Power consumption divided by 4,
- System density increased by 4
SoC ATE revolutionary architecture

- Revolutionary tester architecture
  - 100% ATE high end standard, FPGA based
    - No performance compromise with state of the art ATE
    - Programmable / upgradable / customizable
  - Massively parallel approach
    - One FPGA controls up to 64 channels
    - Big memories (pattern & capture) distributed over many channels

Cost effective, high performance, low power, high density test platform

- Open, flexible, powerful, easy to use interface
  - Windows based Graphical User Interface (GUI) & C++ programming
  - Full Application Programming mixed in templates and / or source code
  - Full debug features: fail list, waveform display, pattern display…
  - 2/3 days full training, 5 min start, few hours test program development

Fast learning, quick programming with keep it simple concepts
High performance SoC ATE for low entry cost

M-Platform modules / features overview  Q1 / 2014

Electro-mechanical structures

- M-5S
- M-21S

Test instruments

- M-D864/1632
- M-MiXW
- M-D148
- M-GTW
- M-DPS10
- M-CBitmap
- M-ClImager

Software

- MuTool
- STIL
- LabVIEW
High performance SoC ATE for low entry cost

- Same test instruments hardware for full compatibility & test program reuse
- Progressive & smooth hardware & firmware upgrades with evolutive configurations and universal slots

GPIB Link

Gbps Ethernet Link

e.g. Oscilloscope

M-5S

Host PC

M-19S with manipulator on prober

Engineering: characterization, failure analysis, IP & chip test validation

Mass production on prober & handler

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3. Reprogrammable System Hardware Application
Digital instrument M-D864
FPGA IP add on
SoC ATE Test Challenge

- DUT generates huge amount of data in a few milliseconds
- Data streams 60 bit packets each, in non deterministic mode
- Each data frame have to be qualified in order to keep only valid ones

Traditional way of the conventional ATE

- huge volume of data have to be captured and requires large capture memory
- Test time impact due to upload of large captures and overall data processing
- Not able to serve real time protocol for the DUT

- Disadvantage: It is not a functional Test !!! Long Test Time

Way of the FPGA based reprogrammable ATE

- huge volume of data are real time evaluated and processed 'on the fly'
- The DUT interface is served by real time protocol at speed
- Small volume of valid data were captured
- No impact to test time

- Advantage: Real Time
ATE Digital Instrument M-D864 basic features

- 64 channels @ 800Mb/s medium to high end digital data rate
  - True differential I/Os improving accuracy
- 32 Mvector / channel (optional: 256 Mvector / channel)
  - Deep memories (pattern, scan and capture)
- 4 independent timing generators per channel
- Capture memory with 12.5 Gb/s bandwidth
  - 16 Gb extended capture memory
  - Real time array (memories, sensors…) analysis with capture instrument
  - Enables embedded memory testing
- PMU per pin & dynamic load
- I/O Switching on the fly, source synchronous
- FPGA based controllers and on board reconfigurable memories allow unique client customization
- Roadmap for D 4128 400Mb/s -128 channels and D 4256 400Mb/s -256 channels
**ATE Digital Instrument M-D864 Front End**

- **DHI** – Drive High
- **DINH** – Drive INhibit
- **VTT** – Tristate Voltage
- **VHH** – Voltage Source
- **DRH** – Driver High Level
- **VTERM** – Termination Voltage
- **DRL** – Driver Low Level
- **DRHCLAMP** – Driver High Clamp Voltage
- **DRLCLAMP** – Driver Low Clamp Voltage
- **KTC** – Test Channel Connect
- **KTC&LD** – Test Channels Dynamic Load Connect
- **KPMUF** – Parametric Measurement Unit Force Connect
- **KPMUS** – Parametric Measurement Unit Sense Connect
- **IOH** – Current Output High
- **IOL** – Current Output Low
- **PGLD** – Programmable Load
- **CRH** – Compare High
- **CRL** – Compare Low
- **CLPH** – Compare Level PMU High
- **KPMU** – PMU Connect
- **FV** – Force Voltage
- **MV** – Measure Voltage
- **SENSE_EXT** – External Sense
- **PMUPPHREF** – Parametric Measurement Unit Per Pin High Reference
- **PMUPPLREF** – Parametric Measurement Unit Per Pin Low Reference
100Mbps data transfer rate
64 bit one Data packet
Non deterministic

(1): The DUT sends its output to the test system

(2): The comparators (only one shown here) translates the electrical level into a Hi/Lo/Z information, which passes through the de-skew and timing delay line

(3): Into the controller, the following block treat the DUT serial stream up to the capture memory module:

The compare logic receives the DUT data and expected data. On real time, it compares expected to DUT and generates a Pass/Fail information. Depending on the mode, it can also simply pass the DUT High/Low state to the following block

The capture logic performs a mask on the DUT information. It filters some cycles, depending on user requirement

Capture from all channel are send to the memory manager which stores the information from some channels to the external memory module. No mechanism to store DUT data into capture memory based on DUT behavior decoding
ATE M-D864 Digital Instrument Dataflow – add on

(1): Block detector – receives a serial data stream which pushes in a shifter and ends with data word (96bit e.c.). The words is compared real time with a mask which defines start/stop. The start/stop words are programmable (up to 4 bits) and data. If start/stop is detected, the packet has to be validated.

(2): Packet Valid detector – a dual NOR/NAND stage compares the received word with a mask which was loaded prior test execution Only valid packets pass to the next stage.

(3): Store logic stage – tells which bits are to be stored when valid packet is detected. This minimizes the number of streams stored and uploaded.

(4): Parallel to serial – the data to be stored. This stage is inserted to rout only one stream to the memory manger to minimize design change of the module.

Other added functions:

Sweep function - An Inc(rement) function has added to 4 differential channels. The Inc of the delay line has 72 ps resolution. This allows to vary the phase of DUT reference clock.

Max frequency – the design runs with 200 MHz - 400 Mbits but up to 800 Mbit is possible

Multi protocol version – at first stage one protocol was handled, but the structure is ready to run different protocol
Advantages of reprogrammable FPGA Hardware:

- ATE is able to react real time on the behavior of the DUT
- Digital instrument is able to run bidirectional protocol
- Solid state machines can be defined with IP cores
- Hardware IP cores are managed in library
- FPGA based controllers and on board reconfigurable memories allow unique test application and client customization

Final Goal:

- Open FPGA area for uploading customer IP core (Q2/2015)
- Customer receives design flow to implement own IP cores
- ‘Hardware’ functional module library
  - Protocol interface library (SPI, CAN, LIN … etc.)
  - Functions library (CRC etc.)
  - DUT specific hardware for real time functional test
Thank You!